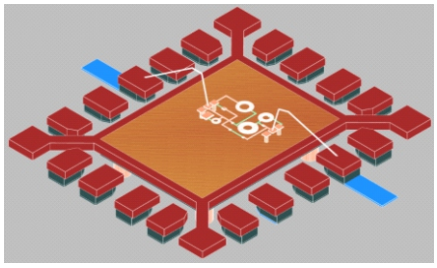
IC and Package Co-Simulation

Faraday Dynamics EDA Solutions

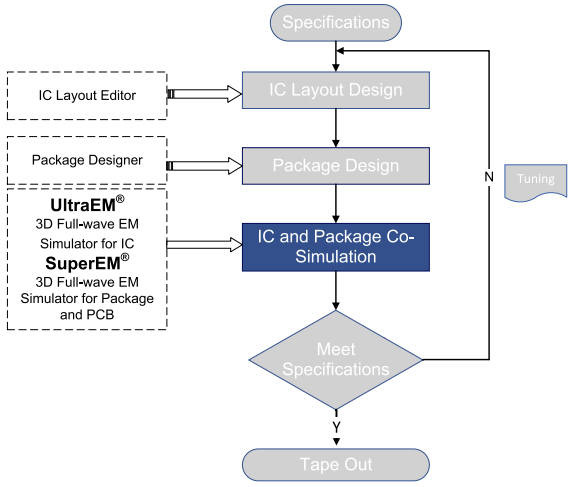
Faraday Dynamics

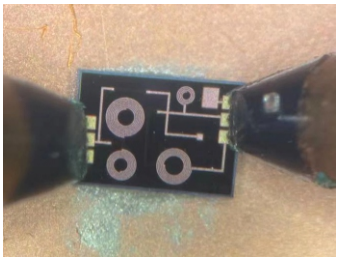
Introduction



Traditionally, chip design and package design are developed separately by different engineering teams. It imposes considerable iteration time and high communication costs. Faraday Dynamics® has developed a unique chip and package co-simulation flow. It provides easy-to-use 3D modeling capability and a specially designed simulation solver for co-simulation, which can reduce the number of iterations; improve the design success rate; and enable chip engineers to assess the package performance at any time during the design process.This reference case demonstrates the co-simulation task of a 5G bandpass filter design using a gallium arsenide process that operates at a frequency range from 3.3GHz to 4.2GHz, a center frequency of 3.8GHz.

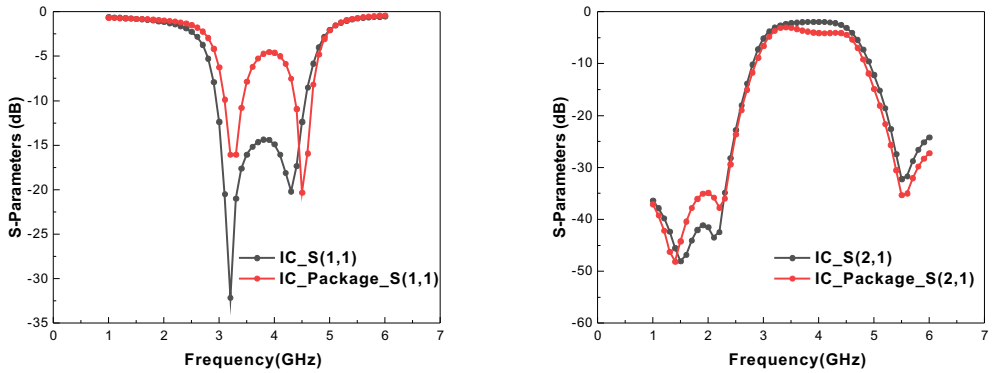
Design Flow





The bandpass filter is designed to operate at a frequency range from 3.3GH to 4.2GHz with a center frequency of 3.8GHz, and a maximum passband attenuation of -2dB. The filter is housed in a QFN package that connects the IC die to a PC board by Bonding Wires. This packaging is used for its good electrical & thermal performance, small footprint size, and lightweight.

Simulation Results



Comparison of Chip-Only vs. Chip-Package Return Loss and Insertion Loss Results

The chip-only and chip-with-package scenarios are simulated to analyze the effect of the package on the filter. The comparison of results shows that the chip-with-package center frequency and passband characteristics are almost the same as the chip-only case. However, the chip-with-package passband maximum attenuation has changed from -2dB to -4dB. With the co-simulation, we can conclude that further chip design refinement must be done to meet the original design target.

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